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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,474	06/25/2001	Matthew J. Amatangelo	AUS920010049US1	8686

35236 7590 11/18/2004

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,474	AMATANGELO ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/2001, 9/17/20*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-18 of U.S. Application 09/888,474 filed on 6/25/2001 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. The prior art used for these rejections is as follows:

4. Teene, A., U.S. Patent 6,272,668. (Henceforth referred to as "**Teene**").

5. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

6. **Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Teene.**

7. In regards to Claim 1, Teene teaches the following limitations:

   1. A method for analyzing an electronic circuit, the method comprising steps of:

   (a) replacing at least one timing determinant block in a first functional

component of the circuit with a timing element set;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.11 lines 63-67 teach that "Finally, element 410 operates to swap standard cell components in the ASIC layout for functionally equivalent standard cell circuit components which optimally improves the timing slack value on each timing arc in the sorted list of timing arcs."

(b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.15, lines 37 to 43 teach that "Element 706 computes temporary variables SLACK and NEWSLACK to the timing slack value for the current timing arc entry. These temporary variables are used in the analysis of each possible functionally equivalent standard cell circuit component to determine which (if any) most improves the timing slack for the timing arc of the current entry."

(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the first functional component; and
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.16, lines 5-7 teach that "Elements 712-714 compute two temporary values used to evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the current cell."

(d) performing a state timing analysis for the circuit utilizing the timing model for the first functional component.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.16, lines 7-15 teach that "DT is the difference in timing slack if the equivalent cell were swapped for the current cell and DS is the new timing slack value if the equivalent cell were swapped for the current cell."

8. In regards to Claim 2, Teene teaches the following limitations:

2. The method of Claim 1 further comprising the step of:
(a) identifying an additional functional component from the circuit to be analyzed.

(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.11 lines 63-67 teach that "Finally, element 410 operates to swap standard cell components in the ASIC layout for functionally equivalent standard cell circuit components which optimally improves the timing slack value on each timing arc in the sorted list of timing arcs."

9. In regards to Claim 3, Teene teaches the following limitations:

3. The method of Claim 2 further comprising the steps of:

(a) replacing at least one timing determinant block in the additional functional component with an additional timing element set;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.11 lines 63-67 teach that "Finally, element 410 operates to swap standard cell components in the ASIC layout for functionally equivalent standard cell circuit components which optimally improves the timing slack value on each timing arc in the sorted list of timing arcs."

(b) performing a circuit simulation for a cross-section of the additional functional component to determine the timing characteristics associated with each replaced timing determinant block of the additional functional component;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.15, lines 37 to 43 teach that "Element 706 computes temporary variables SLACK and NEWSLACK to the timing slack value for the current timing arc entry. These temporary variables are used in the analysis of each possible functionally equivalent standard cell circuit component to determine which (if any) most improves the timing slack for the timing arc of the current entry."

(c) attaching the timing characteristics associated with each replaced timing determinant block of the additional functional component to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the additional functional component; and
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.16, lines 5-7 teach that "Elements 712-714 compute two temporary values used to evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the current cell."

(d) wherein the step of performing a static timing analysis for the circuit also

utilizes the timing model for the additional functional component.
(Teene, especially: col.6, lines 18-34; and col.3, line 18 to col.4, line 65)

10. In regards to Claim 4, Teene teaches the following limitations:

4. The method of Claim 1 further including the step of :

(a) selecting the cross-section of the first functional component to produce a worst-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross timing violations, critical paths, etc., for both worst-case and best-case conditions (process, temperature, and voltage, plus the effect of estimated power dissipation).

11. In regards to Claim 5, Teene teaches the following limitations:

5. The method of Claim 1 further including the step of:

(a) selecting the cross-section of the first functional component to produce a best-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross timing violations, critical paths, etc., for both worst-case and best-case conditions (process, temperature, and voltage, plus the effect of estimated power dissipation).

12. In regards to Claim 6, Teene teaches the following limitations:

6. The method of Claim 1 further including the step of:

(a) developing a group of timing elements for use in producing timing element sets suitable for replacing a number of different timing determinant blocks .
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

13. In regards to Claim 7, Teene teaches the following limitations:

7. The method of Claim 1 wherein each timing determinant block in the first functional component is replaced with a respective tuning element set.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

14. In regards to Claim 8, Teene teaches the following limitations:

8. A method of producing a timing model for use in static timing analysis for an electronic circuit, the method comprising the steps of :

(a) replacing at least one timing determinant block in a functional component of the circuit with a timing element set;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.11 lines 63-67 teach that "Finally, element 410 operates to swap standard cell components in the ASIC layout for functionally equivalent standard cell circuit components which optimally improves the timing slack value on each timing arc in the sorted list of timing arcs."

(b) performing a circuit simulation for a cross-section of the functional component to determine timing characteristics associated with each replaced timing determinant block of the functional component; and
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.15, lines 37 to 43 teach that "Element 706 computes temporary variables SLACK and NEWSLACK to the timing slack value for the current timing arc entry. These temporary variables are used in the analysis of each possible functionally equivalent standard cell circuit component to determine which (if any) most improves the timing slack for the timing arc of the current entry."

(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective tuning determinant block.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.16, lines 5-7 teach that "Elements 712-714 compute two temporary values used to evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the current cell."

15. In regards to Claim 9, Teene teaches the following limitations:

9. The method of Claim 8 further including the step of :
(a) selecting the cross-section of the functional component to produce a worst-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross timing violations, critical paths, etc., for both worst-case and best-case conditions

(process, temperature, and voltage, plus the effect of estimated power dissipation).

16. In regards to Claim 10, Teene teaches the following limitations:

10. The method of Claim 8 further including the step of:
(a) selecting the cross-section Of the first functional component to produce a best-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross timing violations, critical paths, etc., for both worst-case and best-case conditions (process, temperature, and voltage, plus the effect of estimated power dissipation).

17. In regards to Claim 11, Teene teaches the following limitations:

11. The method of Claim 8 further including the step of :
(a) developing a group of timing elements for use in producing timing element sets suitable for replacing a number of different timing determinant blocks.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

18. In regards to Claim 12, Teene teaches the following limitations:

12. The method of Claim 8 wherein each timing determinant block in the functional component is replaced with a respective timing element set.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

19. In regards to Claim 13, Teene teaches the following limitations:

13. The method of Claim 8 wherein the cross-section for the circuit simulation is selected to provide information on a first signal path through the functional component and further including the step of performing a second circuit simulation for a different cross-section of the functional component to determine timing characteristics associated with each replaced timing determinant block of the functional component for that different cross-section.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

20. In regards to Claim 14, Teene teaches the following limitations:

14. A method for employing timing elements to create a timing model for a functional component of a circuit, the method comprising the steps of:

(a) defining a group of timing elements, each timing element in the group

comprising an element for representing at least a portion of the timing characteristics associated with a timing determinant block within the functional component;
(Teene, especially: col.3, lines 1-5)

(b) replacing at least one timing determinant block in the functional component with a timing element set including one or more of the timing elements from the group of timing elements;
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.11 lines 63-67 teach that "Finally, element 410 operates to swap standard cell components in the ASIC layout for functionally equivalent standard cell circuit components which optimally improves the timing slack value on each timing arc in the sorted list of timing arcs."

(c) performing a circuit simulation for a cross-section of the functional component to determine simulated timing characteristics associated with each replaced timing determinant block of the functional component; and
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.15, lines 37 to 43 teach that "Element 706 computes temporary variables SLACK and NEWSLACK to the timing slack value for the current timing arc entry. These temporary variables are used in the analysis of each possible functionally equivalent standard cell circuit component to determine which (if any) most improves the timing slack for the timing arc of the current entry."

(d) attaching the simulated timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Col.16, lines 5-7 teach that "Elements 712-714 compute two temporary values used to evaluate the possible improvement in timing slack caused by swapping the equivalent cell for the current cell."

21. In regards to Claim 15, Teene teaches the following limitations:

15. The method of Claim 14 further including the step of:
(a) selecting the cross-section of the functional component to produce a worst-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross

timing violations, critical paths, etc., for both worst-case and best-case conditions (process, temperature, and voltage, plus the effect of estimated power dissipation).

22. In regards to Claim 16, Teene teaches the following limitations:

16. The method of Claim 14 further including the step of:
(a) selecting the cross-section of the first functional component to produce a best-case timing path through the functional component.
(Teene, especially: col.8, line 62 -col.9, line 30 and Figs.2A-2C)

Col.8, line 65 to Col.9, line 3 teaches: "Element 292 performs optional static timing analysis with pre-layout estimated timings. This can quickly reveal gross timing violations, critical paths, etc., for both worst-case and best-case conditions (process, temperature, and voltage, plus the effect of estimated power dissipation).

23. In regards to Claim 17, Teene teaches the following limitations:

17. The method of Claim 14 wherein each timing determinant block in the functional component is replaced with a respective timing element set.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

24. In regards to Claim 18, Teene teaches the following limitations:

18. The method of Claim 14 wherein the cross-section for the circuit simulation is selected to provide information on a first signal path through the functional component and further including the step of performing a second circuit simulation for a different cross-section of the functional component to determine simulated timing characteristics associated with each replaced timing determinant block of the functional component for that different cross-section.
(Teene, especially: col.11, line 60 -col.12, line 41 and Fig.4; col.14, line 31 - col.18, line 64 and Figs.7A-7C)

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

November 15, 2004